Figure 1 Typical Monitor and Insertion Application

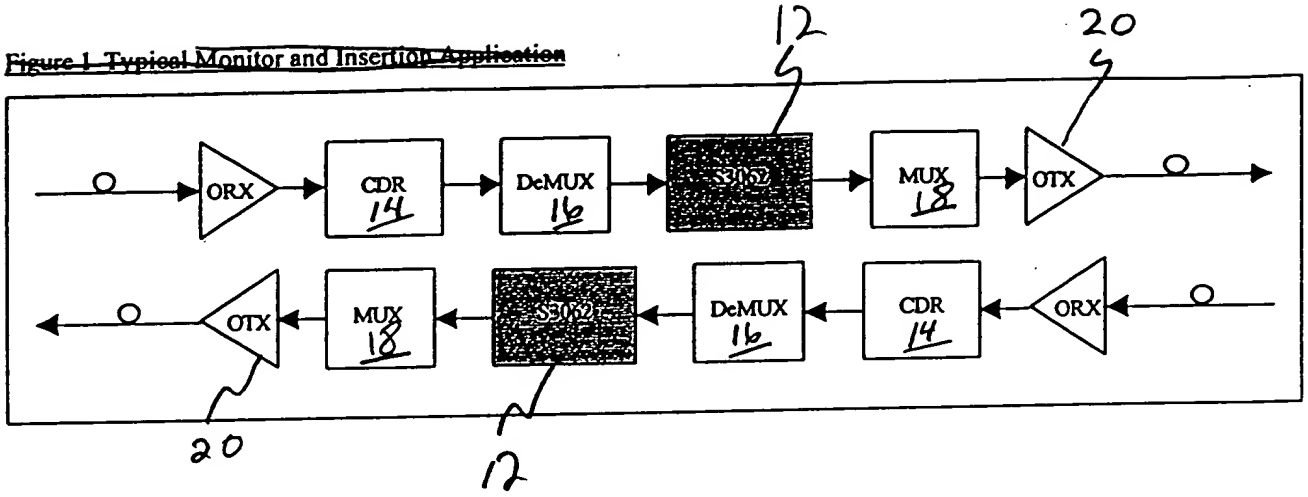

FIG. 1

BEST AVAILABLE COPY

Figure 2 Typical Monitor Application

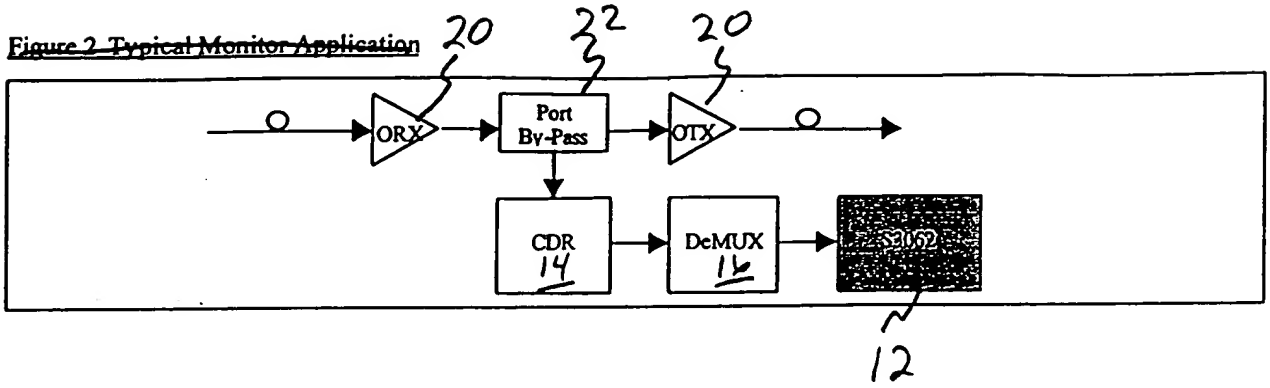

FIG. 2

BEST AVAILABLE COPY

Figure 3 Overview Block Diagram

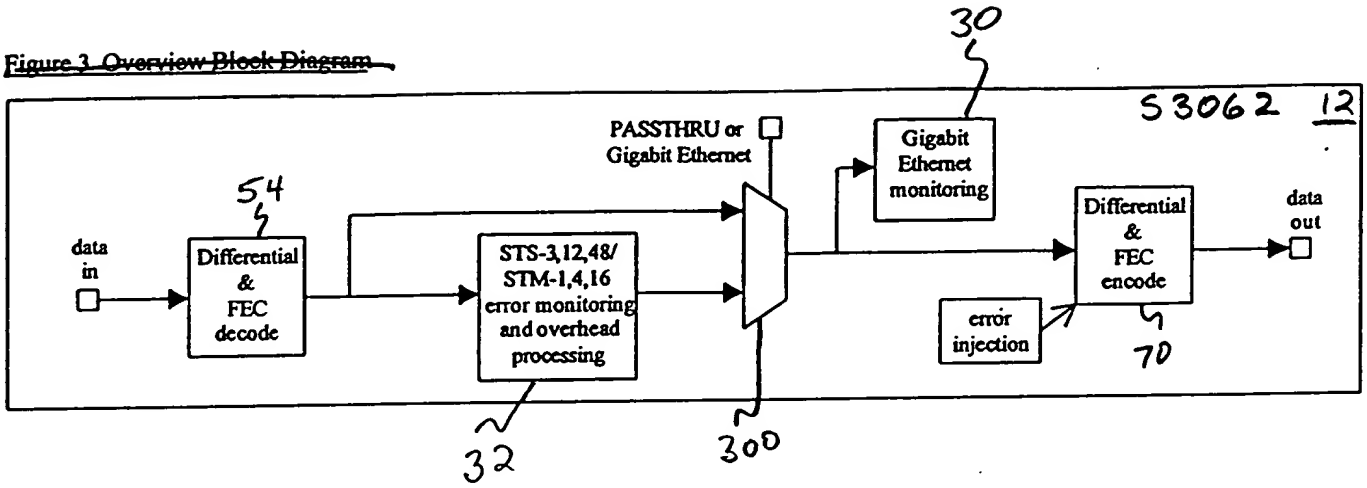

FIG. 3

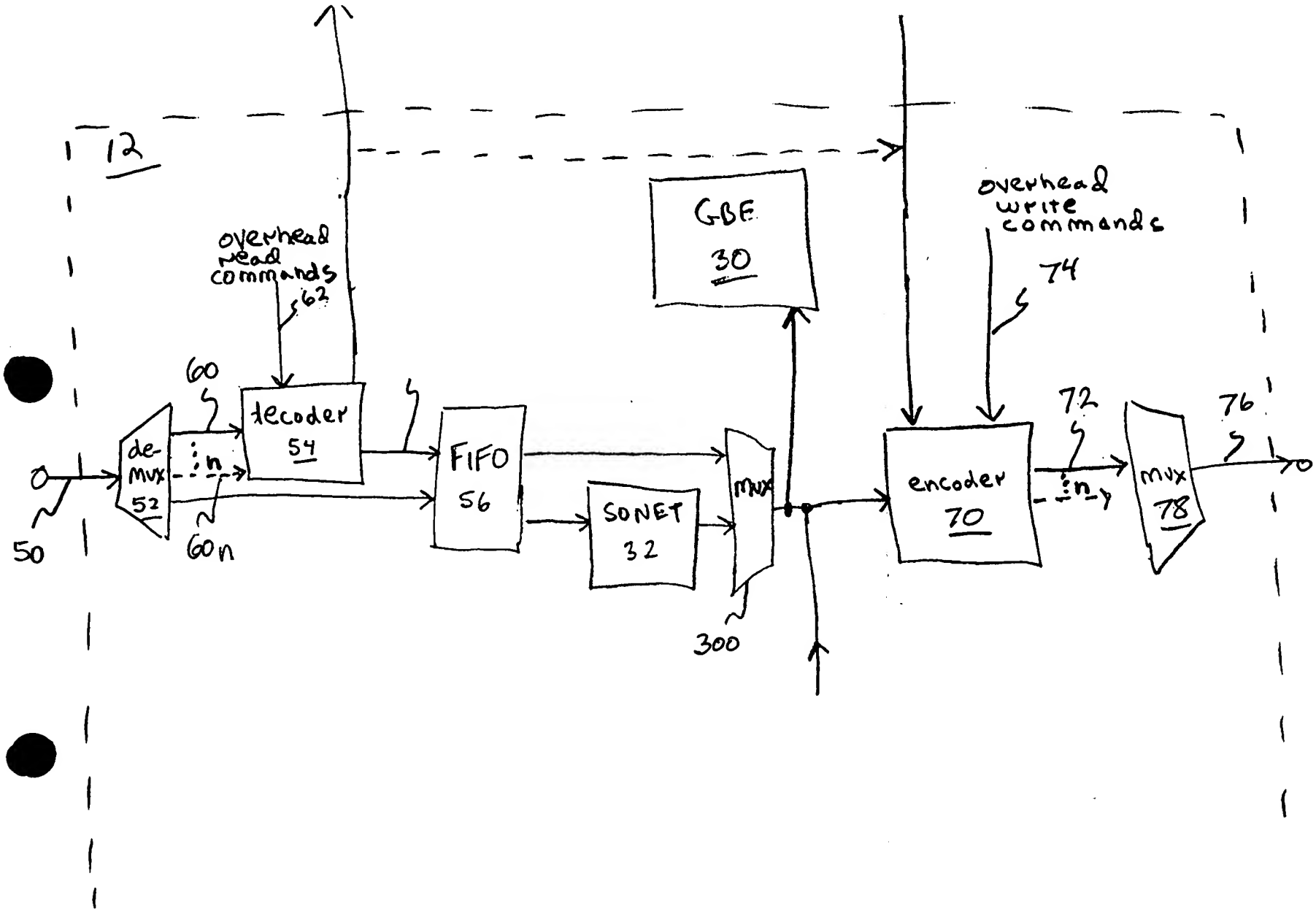

Fig. 4a

09627913 .032700

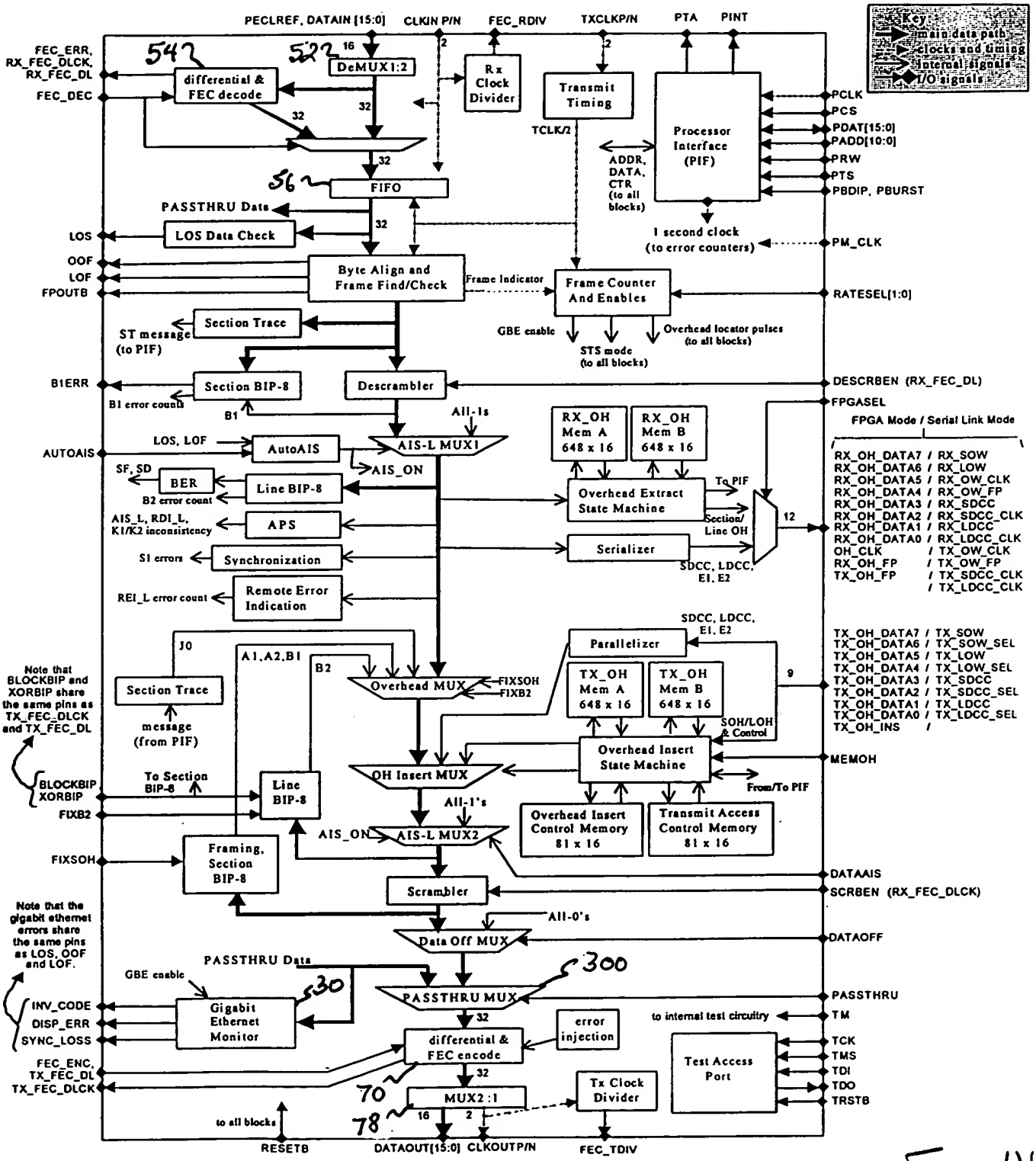

Fig. 46

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~~Figure 6 Data Structure with Forward Error Correction~~

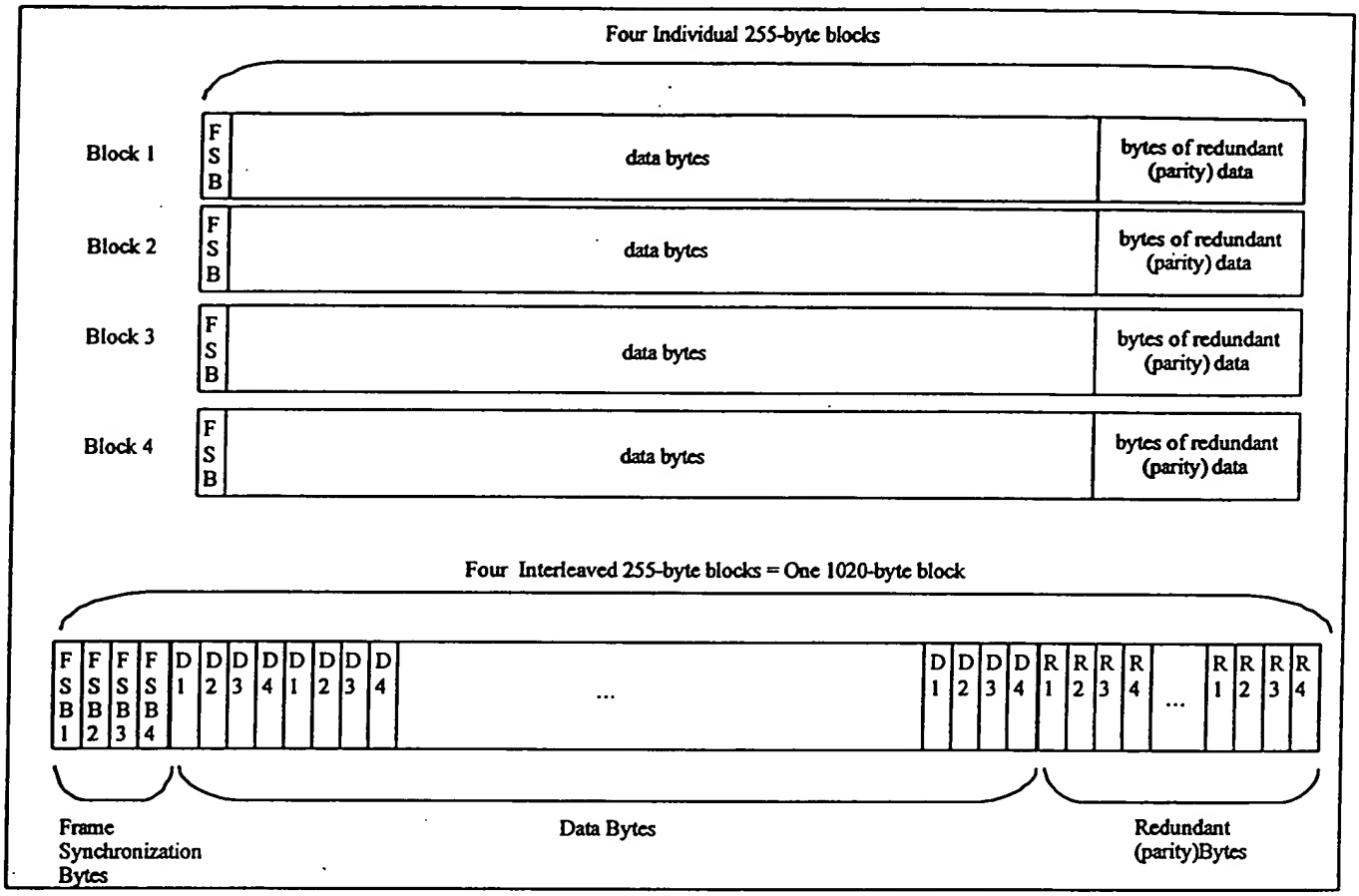


FIG. 5

~~Figure 7 Frame Check Enabling~~

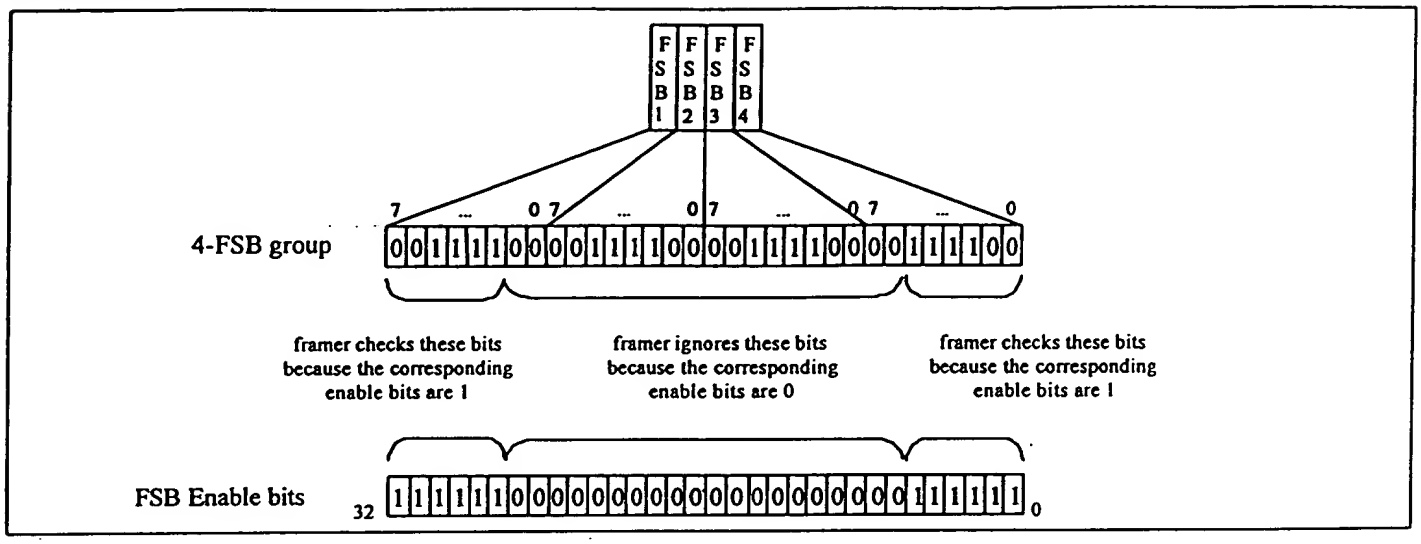


FIG. 6

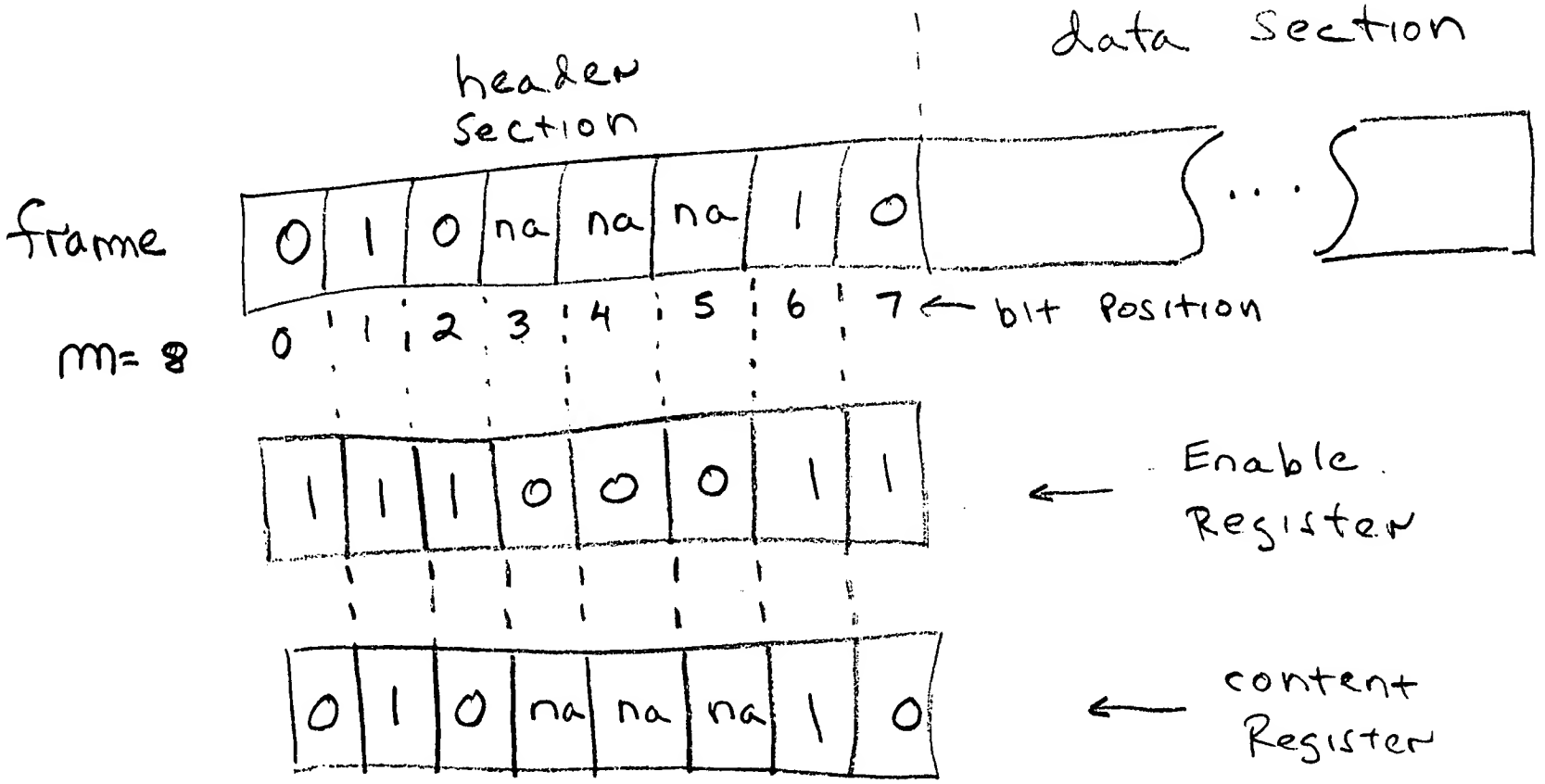
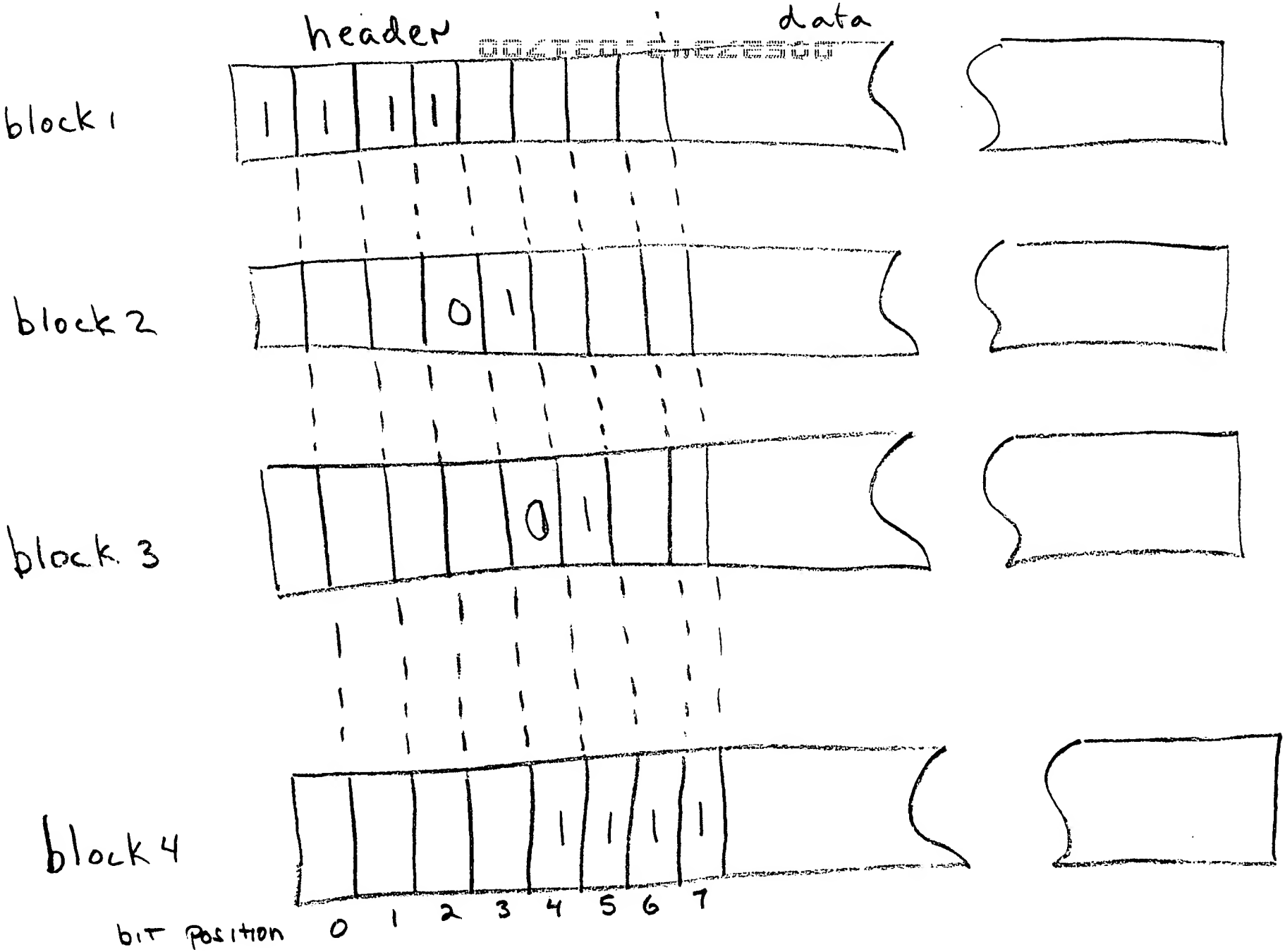

data Section
header Section
frame
0 1 0 na na na 1 0
m= 8
0 1 2 3 4 5 6 7 ← bit Position
1 1 1 0 0 0 1 1
← Enable Register
0 1 0 na na na 1 0
← content Register

Fig. 1


header
data
block 1
1 1 1 1
block 2
0 1
block 3
0 1
block 4
1 1 1 1
bit position 0 1 2 3 4 5 6 7

n = 4
m = 8

Fig. 8

DOCKET CLEARED

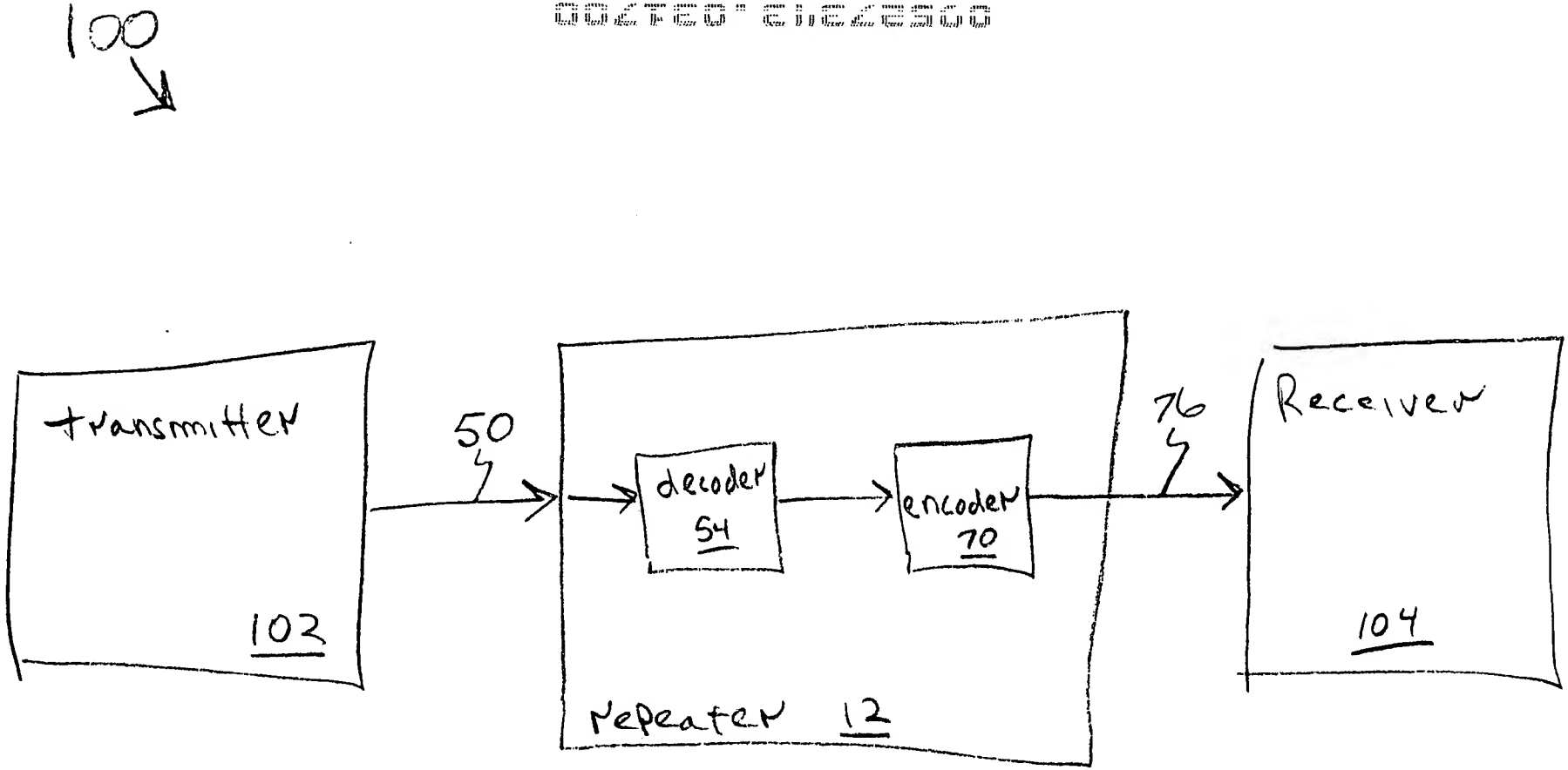


Fig. 9

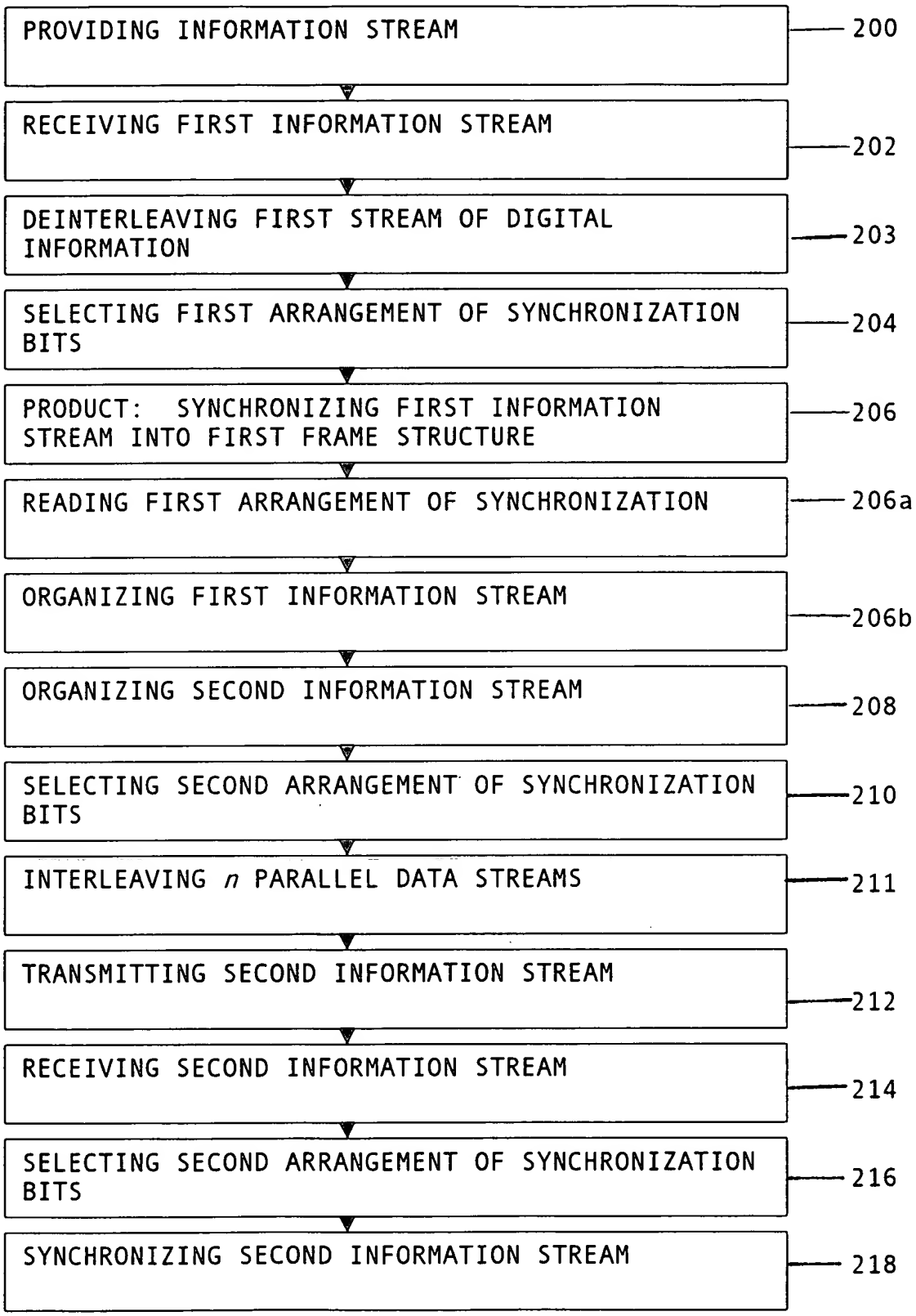

PROVIDING INFORMATION STREAM
200
RECEIVING FIRST INFORMATION STREAM
202
DEINTERLEAVING FIRST STREAM OF DIGITAL INFORMATION
203
SELECTING FIRST ARRANGEMENT OF SYNCHRONIZATION BITS
204
PRODUCT: SYNCHRONIZING FIRST INFORMATION STREAM INTO FIRST FRAME STRUCTURE
206
READING FIRST ARRANGEMENT OF SYNCHRONIZATION
206a
ORGANIZING FIRST INFORMATION STREAM
206b
ORGANIZING SECOND INFORMATION STREAM
208
SELECTING SECOND ARRANGEMENT OF SYNCHRONIZATION BITS
210
INTERLEAVING n PARALLEL DATA STREAMS
211
TRANSMITTING SECOND INFORMATION STREAM
212
RECEIVING SECOND INFORMATION STREAM
214
SELECTING SECOND ARRANGEMENT OF SYNCHRONIZATION BITS
216
SYNCHRONIZING SECOND INFORMATION STREAM
218

FIG. 10

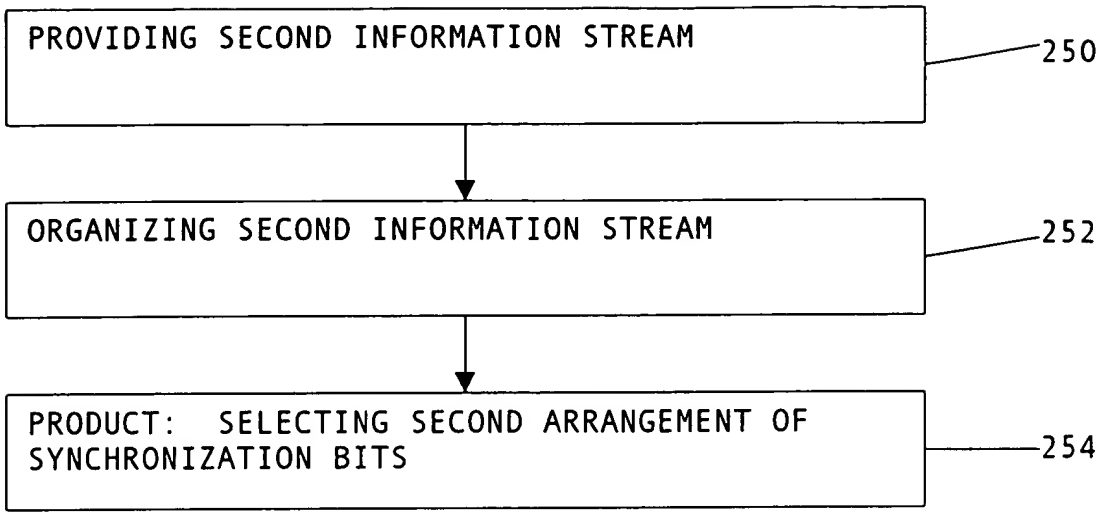

PROVIDING SECOND INFORMATION STREAM
250
ORGANIZING SECOND INFORMATION STREAM
252
PRODUCT: SELECTING SECOND ARRANGEMENT OF SYNCHRONIZATION BITS
254

FIG. 11

Figure 8 Forward Error Correction Framing State Machine

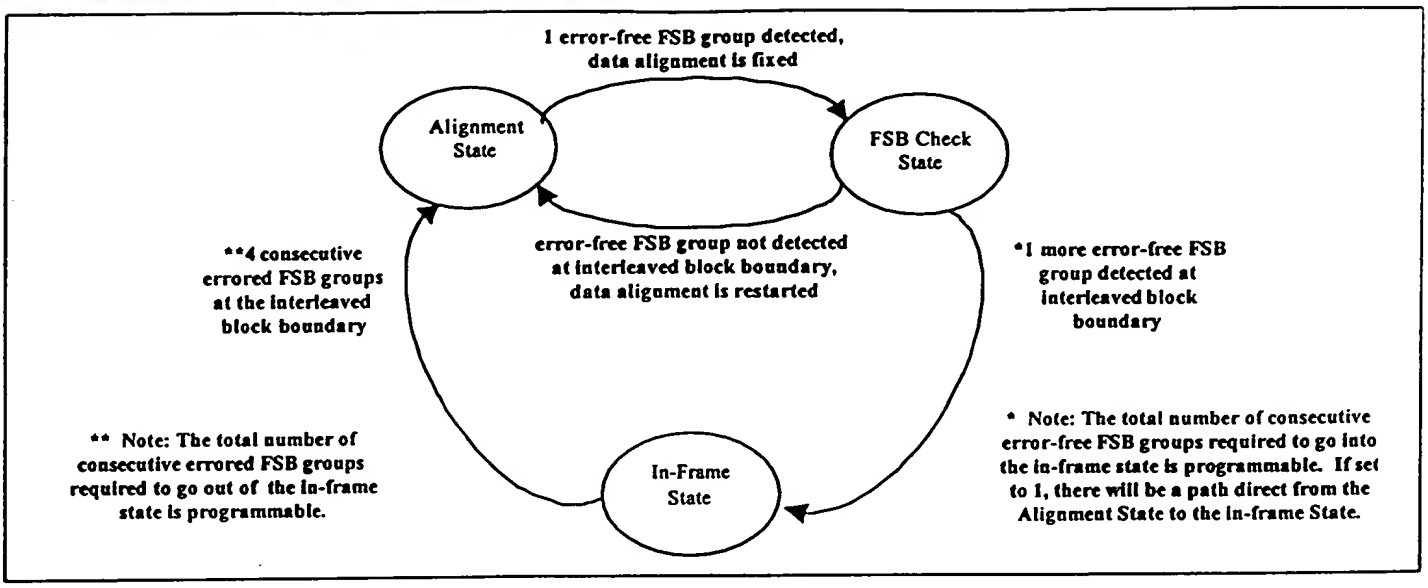


FIG. 12

Figure 10 Required External Circuits for FEC Modes: Both Encode and Decode, or Neither Encode nor Decode

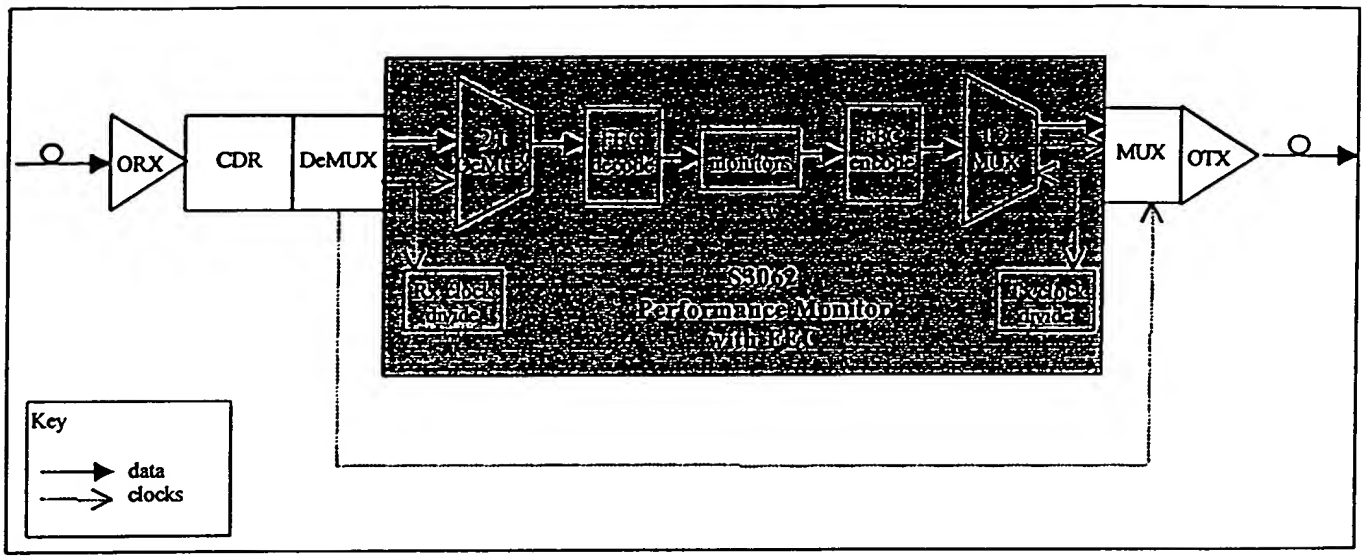


FIG. 13

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~~Figure 11 Gigabit Ethernet Block Diagram~~

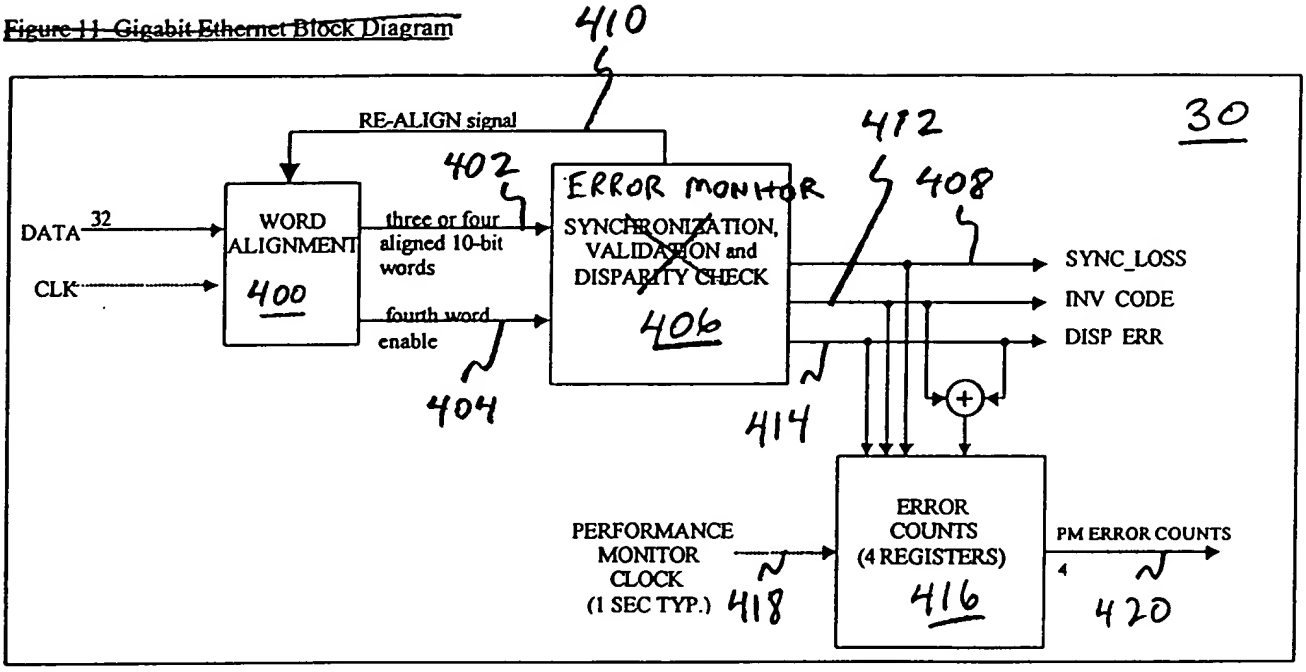

FIG. 14

Figure 12-802.3z RD Column Determination

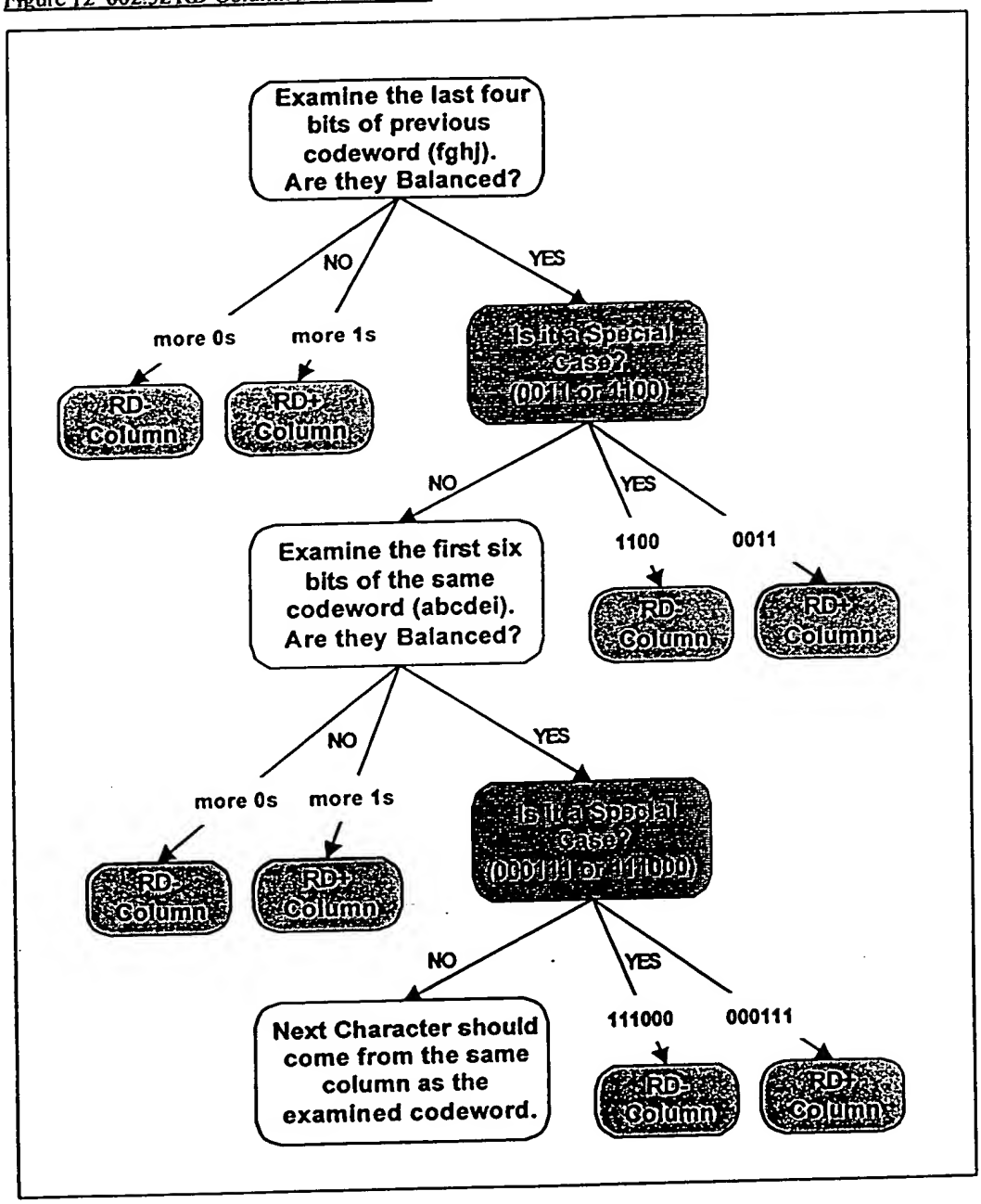

FIG. 15

BEST AVAILABLE COPY

Figure 14 SONET STS-3c and SDH STM-1 Frames Showing the Transport Overhead

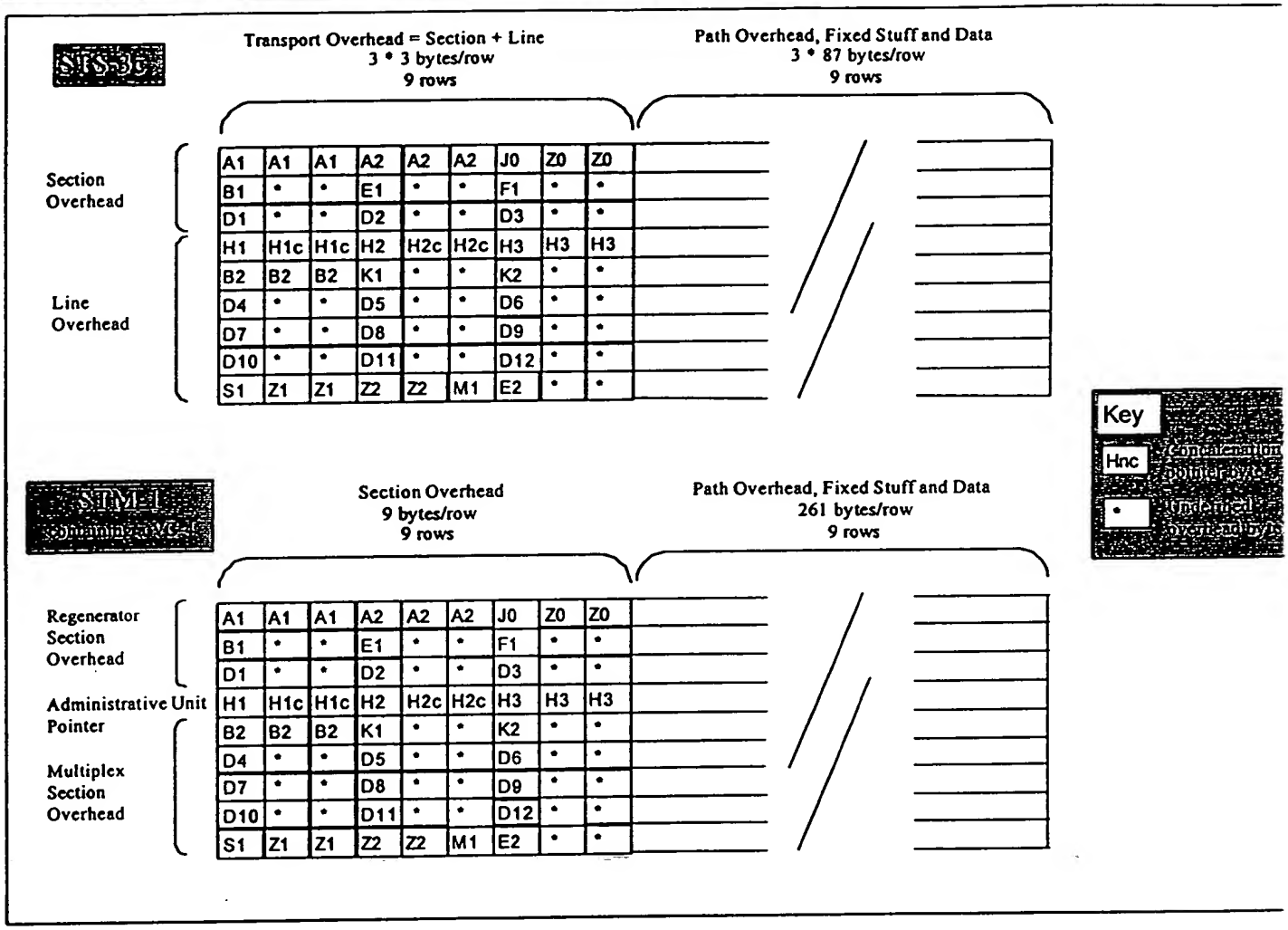

FIG. 16

BEST AVAILABLE COPY

Figure 15 SONET STS-Nc and SDH STM-N Frames Showing the Transport Overhead

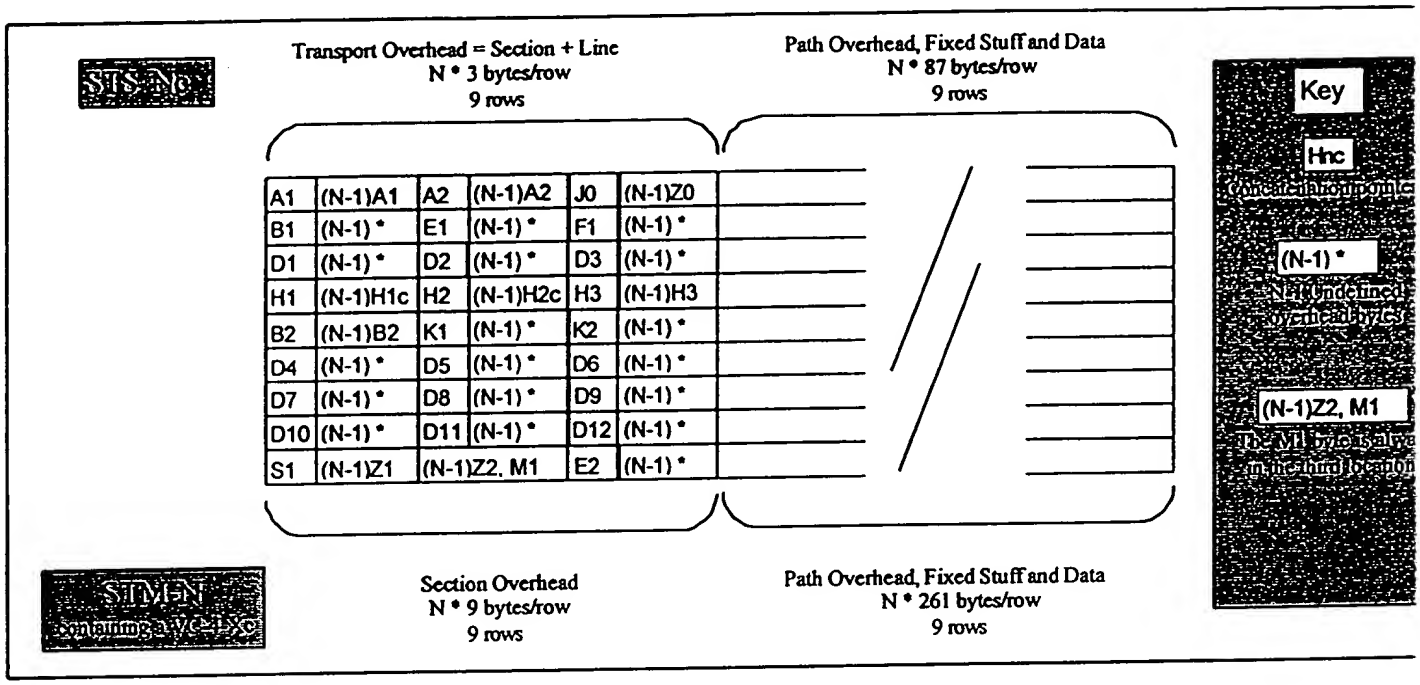

FIG. 17

BEST AVAILABLE COPY

Figure 17 LOF and OOF (SEF) State Machine Diagram

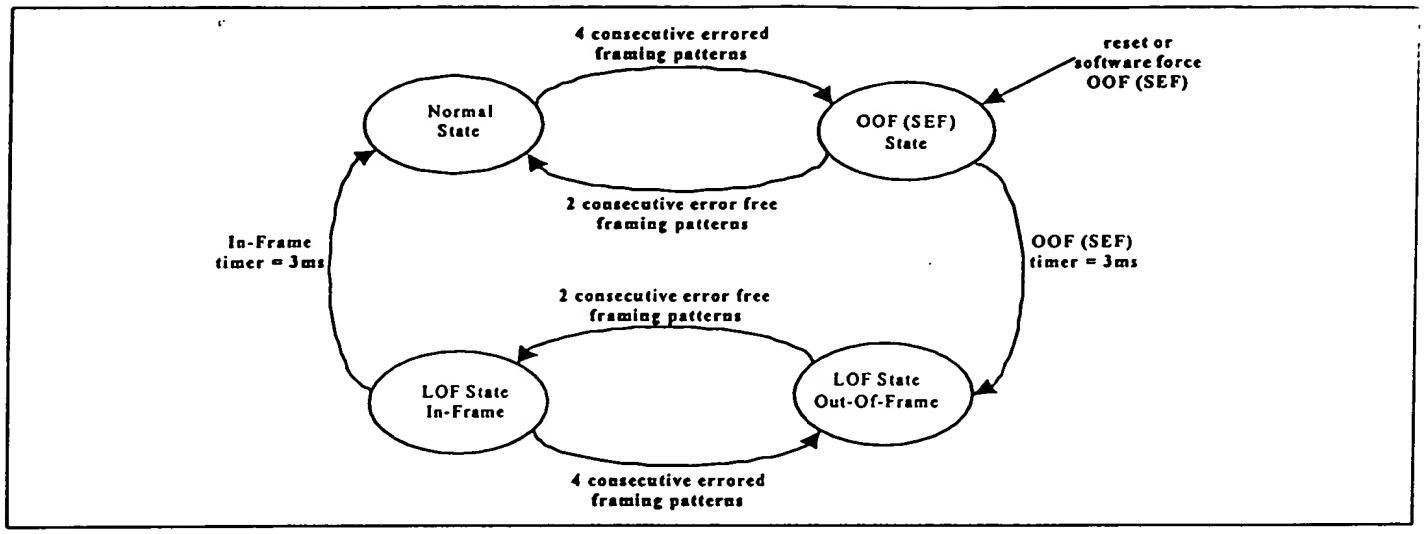

FIG. 18

BEST AVAILABLE COPY

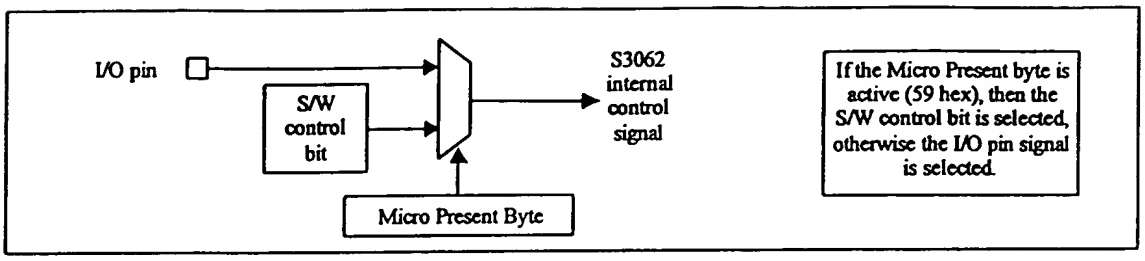
I/O pin
S/W control bit
S3062 internal control signal
Micro Present Byte
If the Micro Present byte is active (59 hex), then the S/W control bit is selected, otherwise the I/O pin signal is selected.

FIG. 19